

## ***XTR300EVM User's Guide***

This user's guide describes the characteristics, operation, and use of the XTR300EVM evaluation module (EVM). This EVM features the XTR300 and has a flexible configuration, allowing for evaluation suitable to a variety of applications.

The following related documents are available through the Texas Instruments web site at [www.ti.com](http://www.ti.com).

**Table 1. Related Documentation  
from Texas Instruments**

DOCUMENT	LITERATURE NUMBER
XTR300 Product Data Sheet	<a href="#">SBOS336</a>
<i>QFN / SON PCB Attachment</i> Application Note	<a href="#">SLUA271</a>
<i>Quad Flatpack No-Lead Logic</i> Packages Application Note	<a href="#">SCBA017</a>

## **1 XTR300 and XTR300EVM Overview**

### **1.1 XTR300**

The XTR300 is a complete output driver for industrial and process control applications. The XTR300 can be configured for current ( $\pm 20\text{mA}$ ) or voltage ( $\pm 10\text{V}$ ) output through pins M1 and M2. No external shunt resistor is required. Only external gain-setting resistors and a loop compensation capacitor are required.

The XTR300 offers separate driver and receiver channels for improved flexibility. The internal instrumentation amplifier (IA) is normally connected for remote voltage sensing in voltage output mode. Alternatively, it can be used as a high voltage, high impedance measurement channel. In voltage output mode, a copy of the output current is provided to allow easy testing of the load condition and eventual calculation of the load resistance. In current output mode, the voltage can be monitored. Using the monitor outputs along with the error flags will provide full test capability of the XTR300 in operation.

Error flags (EF) are provided to indicate fault conditions on the output. These flags indicate:

- a thermal overload condition ( $\text{EF}_{\text{OT}}$ );
- a violation of the common-mode input range of the instrumentation amplifier ( $\text{EF}_{\text{CM}}$ );
- an over-current or short-circuit condition in the load ( $\text{EF}_{\text{LD}}$ ) in voltage output mode, or open or high load resistance in current output mode.

Although the XTR300 is not designed with thermal shutdown, an automatic thermal protection function can be implemented simply by connecting  $\text{EF}_{\text{OT}}$  to OD (requires an external pull-up resistor), disabling the output. This connection is not made internally to allow flexibility in how a system handles an over-temperature condition.

## 1.2 XTR300EVM Overview

The XTR300 EVM is intended to provide basic evaluation of the functionality and performance of the XTR300. The layout is not intended to be a model for the target circuit, nor is it laid out for electromagnetic compatibility (EMC) testing.

The layout of the XTR300EVM printed circuit board (PCB) is designed to provide:

- easy handling of the small QFN package with the recommended land pattern to which the QFN device is soldered. A mechanical drawing of the recommended land pattern is found at the end of the [product datasheet](#). The solder connection includes heat sinking through the exposed thermal die pad of the QFN package to ambient air.
- easy access to all pins of the device.
- space for optional resistors and capacitors, as well as for the required gain-setting resistors and loop compensation capacitor. Components are placed with adequate space, to allow modification and population with SOIC or leaded components.
- resistors in the I/O connections to add additional handling protection for the EVM (which might not be used in the final circuit).
- open space around the IC to allow eventual re-soldering.

The XTR300 is initially configured for a basic setup that allows demonstration of the high precision capability of the XTR300 in both current and voltage output mode, as well as the performance of the instrumentation amplifier in the analog input mode. While the circuit can be modified for other applications, we recommend some testing with the original set-up, because the high precision resistors provided will produce high precision performance. Note that the accuracy of the precision resistors used in the EVM is only 0.1%, whereas the XTR300 has even greater accuracy.

The EVM requires an external supply voltage for the signal path and a logic level supply of 3V to 5V for external pull-up. Refer to the product data sheet for comprehensive information about the XTR300.

## 2 Quick Start Setup and Use

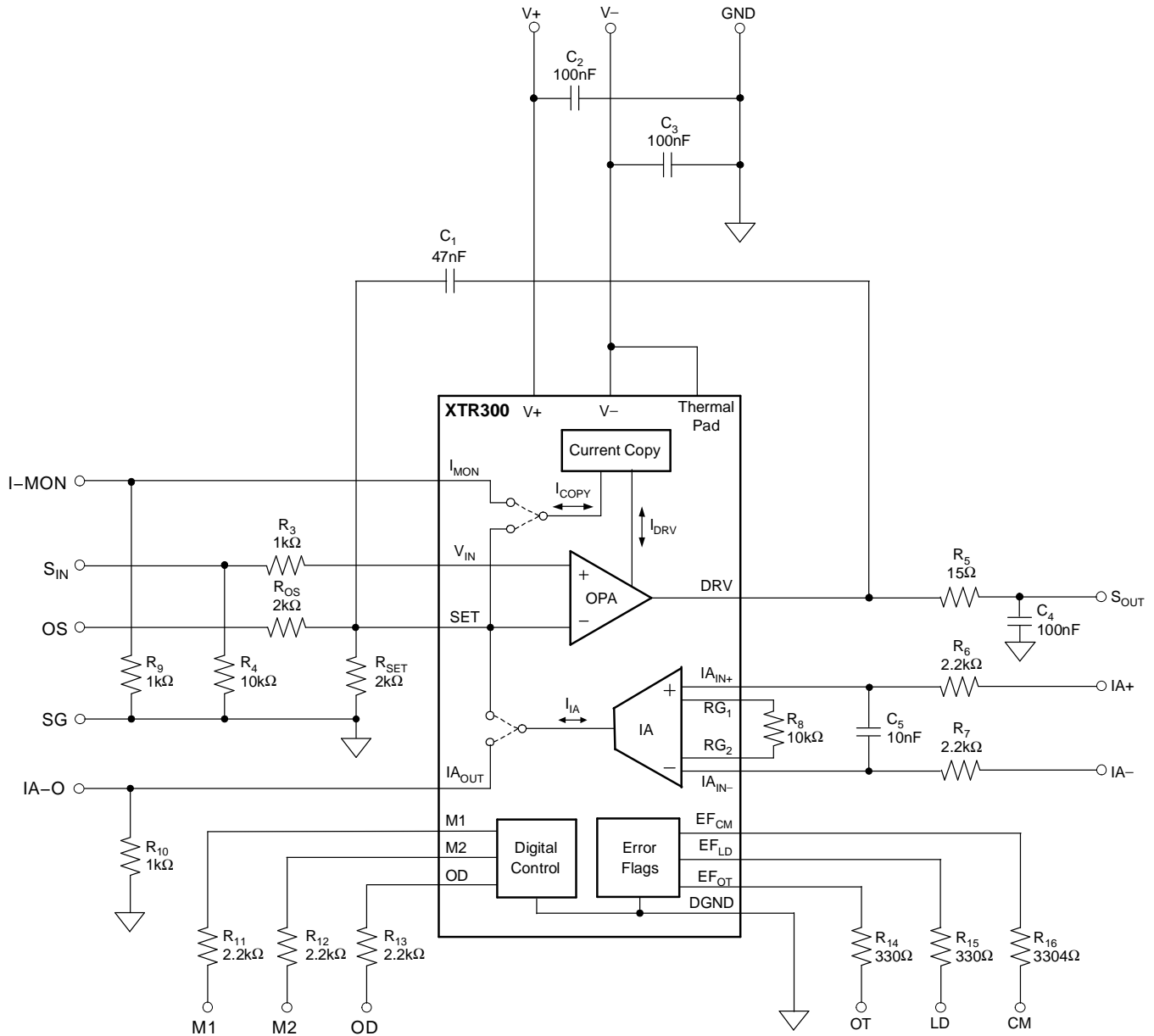
Follow these procedures to set up and use the XTR300EVM. See [Figure 1](#).

- Connect IA+ to S<sub>OUT</sub> and IA– to GND.
- Connect OS (offset shift) to SG (signal ground).
- Connect an external DC supply voltage of ±15V to ±20V to the V+ and V– connector, referenced to the GND connector.
- Turn power on. Expect a supply current of less than 3mA (without load and after charging the bypass capacitors). The S<sub>OUT</sub> pin should stay close to GND with a small amount of offset (use an oscilloscope to observe the output signal).
- Connect a function generator or signal source to the S<sub>IN</sub> connector pin with ground connected to GND or SG. Set amplitude to ±2V<sub>PP</sub> or lower (approximately 100Hz); it should appear at the output with five times the amplitude.
- Without any connection to the mode inputs, the device operates in voltage output mode.

## 3 Circuit Description

### 3.1 Signal Path

The circuit of the EVM is shown in [Figure 1](#). M2 configures the XTR300 for voltage output mode (M1 = L, M2 = L) or current output mode (M1 = L, M2 = H). When using current output mode, a load resistor must be connected to S<sub>OUT</sub> to provide a current path (to GND). S<sub>OUT</sub> can only operate within the specified limits of the supply voltage.



NOTE: The EVM uses one common ground for SG, DGND, and GND. See *Layout and Grounds* for more information.

**Figure 1. XTR300EVM Circuit**

A  $\pm 2V_{PP}$  input signal generates an output voltage of  $\pm 10V_{PP}$  in voltage output mode or an output current of  $\pm 20mA$  in current output mode. The same output signals can be generated from a single-ended 0V to +4V input signal with OS connected to +4V instead of GND.

A large capacitor for  $C_1$  is used to reduce the loop bandwidth to normal industrial requirements. The input of the instrumentation amplifier is filtered ( $C_5$  and  $R_6 + R_7$ ) to reject high frequency noise that may be present at the terminals. If a faster signal path is required, both capacitors must be made smaller (or removed).

### 3.2 Digital I/O

The error flags have open collector outputs with an internal pull-up current of only 1 $\mu$ A to 5V. This small current allows the user to observe the error flags with the 10M $\Omega$  scope probe on the EVM. For normal operation with connection to external logic inputs, however, external pull-up resistors are required.

If OT is connected to OD, which enables the automatic thermal protection, an external pull-up resistor is required for proper operation and noise rejection.

The resistors in the digital I/O of this EVM add additional protection (current limit). They are optional or can be resized in the final circuit. The sink current of the digital outputs can be as much as 5mA to drive an LED or optical-coupler. Resistors R<sub>14</sub>, R<sub>15</sub> and R<sub>16</sub> are used to set the current.

### 3.3 Monitor Outputs

In voltage output mode, the signal output current can be observed and measured at I-MON with 0.1V/mA (with R<sub>9</sub> = 1k $\Omega$ ).

In current output mode, the signal output voltage can be observed and measured at IA-O with 0.2V/V (with R<sub>10</sub> = 1k $\Omega$ ).

These output pins can be connected together to form a general monitor output, because they are internally multiplexed (**Note:** R<sub>9</sub> and R<sub>10</sub> appear in parallel).

### 3.4 Signal Output

R<sub>5</sub> provides some current limitation into the protection cell of the DRV pin if back-driven from the output. External clamp diodes (standard diodes) are recommended from supply to the S<sub>OUT</sub> connection. For more details, see the [product data sheet](#).

### 3.5 Layout and Grounds

The XTR300EVM has three grounds connected together:

- Signal input ground (SG): the reference point for the input signal and monitor outputs.
- Digital reference ground (DGND): the reference point for the digital inputs and current return for the digital outputs.
- Power ground (GND): used for decoupling and reference to the supply.

These grounds, or reference points, can be moved within some range independently; the PCB layout allows disconnecting these grounds by cutting the appropriate trace. However, the grounds must not be allowed to float. Any external voltage connected to one of the (disconnected) grounds must be within the specified operating range (see [product data sheet](#) and observe power-on/off conditions).

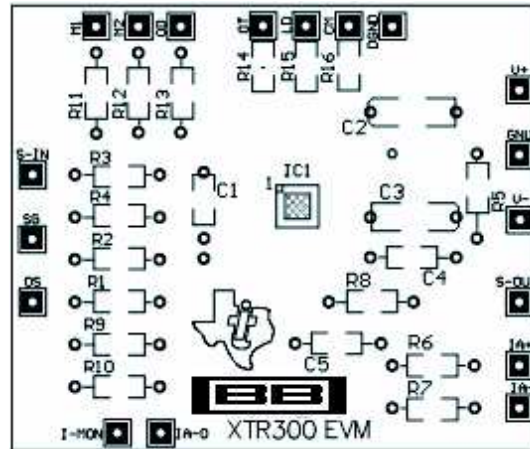
This flexible signal reference ground arrangement of the XTR300 eases circuit layout and offers important flexibility. The supply ground is primarily used for decoupling and connection to the power source and output protection circuitry. The DGND carries the digital load current and can be connected closer to the digital circuitry. The signal ground (SG) is a common node for several resistors to make the EVM easy to use. In the target circuit, however, R<sub>2</sub> can be connected to another signal reference point; for example, to a life zero or DAC midpoint reference.

Both monitor outputs are controlled currents. Therefore, resistors R<sub>9</sub> and R<sub>10</sub> can be referenced to a node useful for signal processing.

Note that the exposed thermal die flag must be connected to the most negative supply.

## 4 Description of Components

This section summarizes the XTR300EVM components. (See also [Figure 2](#).)



**Figure 2. XTR300EVM PCB (Top Layer)**

**R<sub>1</sub> (R<sub>OS</sub>) and R<sub>2</sub> (R<sub>SET</sub>):** These resistors set the gain or transconductance with their parallel resistance. They are split to allow additional signal offset shift (R<sub>1</sub>). If no offset shift is required, only R<sub>2</sub> is used. Both resistors influence drift and DC accuracy.

**R<sub>3</sub>:** This resistor matches the impedance of  $R_2 \parallel R_1$  for approximate cancellation of the bias current.

**R<sub>4</sub>:** This resistor is used for the EVM input to provide a signal reference with no signal source connected.

**R<sub>5</sub> (R<sub>C</sub>):** This resistor provides stability for large capacitive loads together with C<sub>1</sub>, and is part of the output protection.

**R<sub>6</sub> and R<sub>7</sub>:** These resistors are used for protection of the IA inputs. Together with C<sub>5</sub>, they also act as a low-pass filter.

**R<sub>8</sub> (R<sub>GAIN</sub>):** This resistor sets the input gain of the IA. It is normally selected to match the 20mA output with the 10V signal. R<sub>8</sub> also influences drift and DC accuracy together with R<sub>2</sub> and eventually R<sub>1</sub>. Try to avoid long wires and stray capacitance to minimize noise pick up.

**R<sub>9</sub> (R<sub>IMON</sub>) and R<sub>10</sub> (R<sub>IA</sub>):** These resistors convert the monitor output current into voltage. If both monitor outputs are tied together, only one resistor is required. The accuracy and drift of the resistor(s) influences the DC performance of the monitor signal output.

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**Note:** Monitor outputs are controlled current outputs. If the monitor output is not used, connect it to GND directly or through a resistor to provide a current path and allow the internal circuit to remain in the normal operating condition.

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**R<sub>11</sub> through R<sub>16</sub>:** These resistors provide additional protection during evaluation only. They are not required in a final circuit, unless they are needed to set the current for driving an LED or optical coupler.

**C<sub>1</sub> (C<sub>C</sub>):** This capacitor forms a time constant with  $R_1 \parallel R_2$ , and defines the frequency roll-off.

**C<sub>2</sub> and C<sub>3</sub>:** These components are supply bypass capacitors; use 100nF or larger.

**C<sub>4</sub>:** This capacitor is part of the output protection and helps to reduce noise. The size is empirical.

**C<sub>5</sub>:** This capacitor, together with R<sub>6</sub> and R<sub>7</sub>, forms a low-pass filter and so defines the bandwidth. It also protects the instrumentation amplifier from very fast distortion pulses.

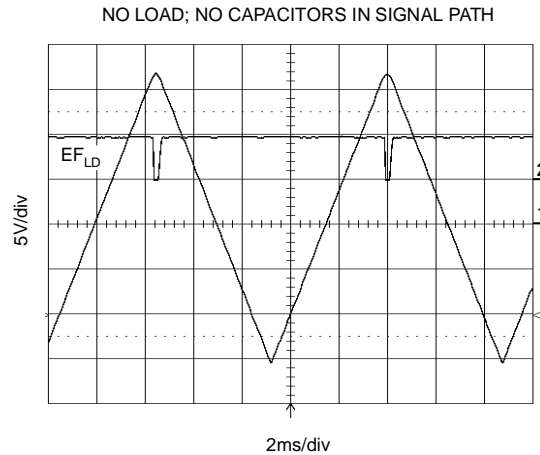
**DGND:** This pin is the ground reference for the digital I/O, and is connected to SG (Signal Ground). If required, this connection could be cut.

**GND:** This trace is the power ground or bypass ground, and is connected to SG; it can be cut at the bottom trace to C<sub>4</sub> or between C<sub>3</sub> and C<sub>4</sub>.

## 5 Scope Photos - Example Traces

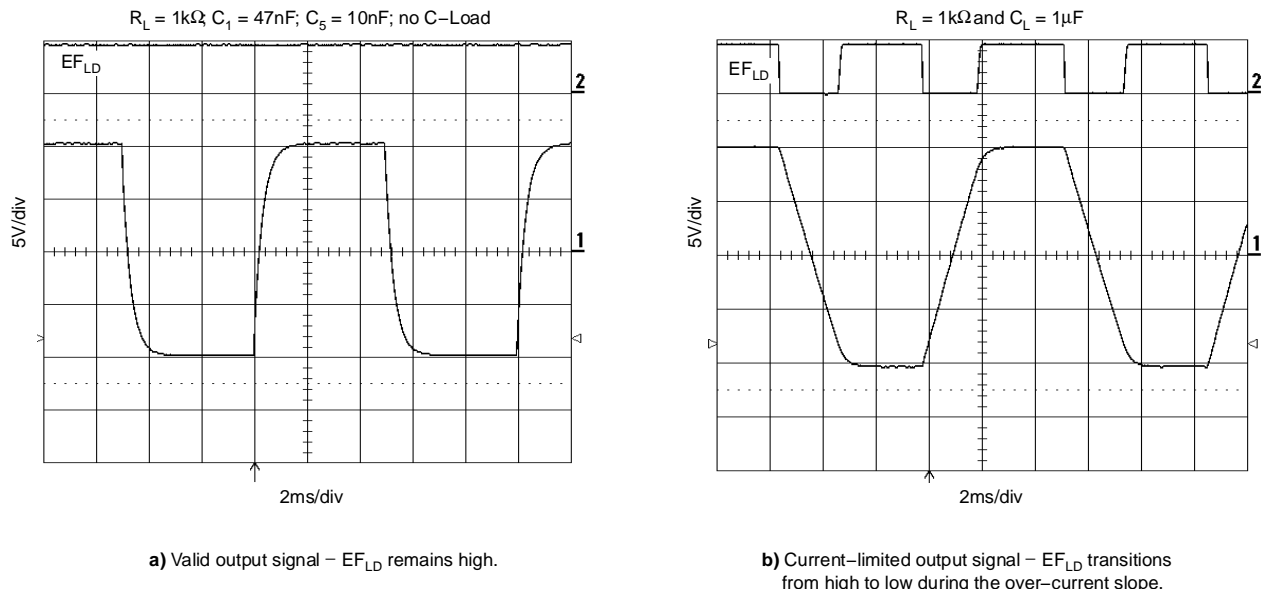
The following scope photos show example traces taken with a digital sampling scope. The test circuit is based on the initial EVM circuit with a supply voltage of  $\pm 18V$ .

**Figure 3** shows the output signal being driven into the rail (channel 1). The signal is not necessarily distorted, but channel 2 shows the error flag,  $EF_{LD}$ , indicating the excursion beyond the linear range. Note that the error flags are asserted low.



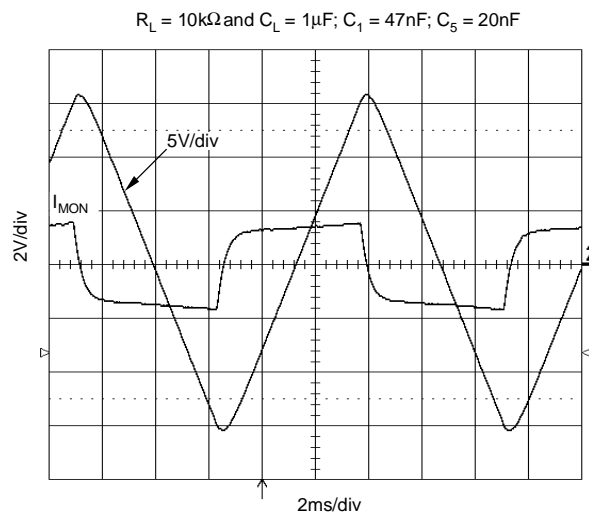
**Figure 3. Error Flag Indicating Output Signal Being Overdriven**

**Figure 4** shows two examples of an output square wave using the circuit of **Figure 1**. In **Figure 4a**, the square wave rise-and-fall time is set by  $C_1$  and  $C_5$  and corresponding resistors. Note that there is no large capacitive load connected; a large capacitive load results in an output signal, as shown in **Figure 4b**. The XTR300 output stage goes into a current limit condition during charge and discharge of the  $1\mu F$  load capacitor. The  $EF_{LD}$  then goes low to indicate that during this slewing condition, the output signal is erroneous.



**Figure 4. High Slew Rate Into Large Capacitive Load Can Drive Output Into Current Limit Mode**

The triangular signal of Figure 5 has a slow enough  $dV/dt$  to maintain the load current within the linear range. The current monitor output shows the load current into the  $1\mu\text{F}$  and  $10\text{k}\Omega$  load. The  $1.8\text{V}_{\text{PP}}$  signal across the  $1\text{k}\Omega$  resistor ( $R_9$ ) translates into  $18\text{mA}$  load current.



**Figure 5. Current Monitor Signal While Driving R/C-Load**

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of  $\leq 44V$  total and the output voltage range of  $\leq 44V$  total.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than  $+125^{\circ}\text{C}$ . The EVM is designed to operate properly with certain components above  $+125^{\circ}\text{C}$  as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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